High-gain differential CMOS transimpedance amplifier with on-chip buried double junction photodiode

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An integrated fully differential CMOS transimpedance amplifier (TIA) with buried double junction photodiode input is described. The TIA features a variable high transimpedance gain ($250\,k\Omega$ to $2.5\,M\Omega$), large DC photocurrent rejection capability (>55 dB) and low input referred noise density at 100 kHz (2pA/√Hz).

Introduction: The transimpedance amplifier (TIA) is widely used in optical receiver circuits. The majority of CMOS TIA designs reported in the literature are intended for high speed digital signal reception. The TIA reported in this Letter is optimised for low noise analogue optical signal detection, in a situation where a weak modulated optical signal is superimposed on a large DC background. This type of signal may be encountered for example in optical coherence tomography (OCT) [1]. Specifically, our design is optimised to detect a 100 kHz carrier frequency, 5 kHz bandwidth signal, and to reject an unwanted DC component with 50 dB attenuation compared to the signal band gain. Our TIA differs from other similar designs [2, 3] through the unique combination of an on-chip buried double junction (BDJ) photodiode, very high adjustable gain and attendant low noise.

Circuit description: A block diagram of the differential TIA is shown in Fig. 1. The circuit has three main parts: input stage, transimpedance stage and feedback DC rejection stage. The input stage includes a BDJ [4] photodiode and associated circuitry. A cross-section of the BDJ photodiode is shown in Fig. 2. A 60 by 60 μm P+–N-well junction forms the P+–N-well photodiode. The N-well and P-substrate junction forms the P-sub/N-well photodiode. As shown in Fig. 1, the photocurrent of the P+–N-well photodiode is $I_{D1} + I_{D2}$, where $I_{D1}$ is AC signal and $I_{D2}$ is DC background, similarly the photocurrent of the P-sub/N-well is $I_{D2}$. The common-mode feedback (CMFB) circuit senses the common-mode voltage at the input to the transimpedance stage and creates an amplified error signal (relative to a 0 V reference) that controls two identical current sources. The current sources then drive the common-mode voltage to zero. In the steady state, each of the identical current sources has a sources. The current sources then drive the common-mode voltage to small DC to large DC. This type of signal is superimposed on a large DC background. This type of signal may be encountered for example in optical coherence tomography (OCT) [1]. Specifically, our design is optimised to detect a 100 kHz carrier frequency, 5 kHz bandwidth signal, and to reject an unwanted DC component with 50 dB attenuation compared to the signal band gain. Our TIA differs from other similar designs [2, 3] through the unique combination of an on-chip buried double junction (BDJ) photodiode, very high adjustable gain and attendant low noise.

Simulation and measurement: The BSIM3 level 49 transistor model was used in HSPICE simulations of the TIA. Because an accurate flicker noise model is not available, the simulated noise spectrum includes thermal noise only.

The optical receiver (TIA and BDJ photodiode) was fabricated in a 1.5 μm process and supplied with ±3.5 V. In addition to the optical receiver, the fabricated chip also contained an additional BDJ photodiode for responsivity testing at 847 nm. The measured responsivities of the P+–N-well and P-sub/N-well photodiode were 0.036 and 0.186 A/W, respectively. The optical receiver frequency response was measured within the frequency range 30–500 kHz using an optical input signal. At each frequency the TIA gain was computed by dividing the optical receiver gain by the overall BDJ photodiode responsivity. The measured TIA frequency response is shown in Fig. 3, with the TIA gain control voltage set to 1.6 V. The shape of the response and high/low frequency cutoffs are as expected. The peak gain at 100 kHz is 1.1 MΩ. By varying the TIA gain control voltage from 3.5–1.35 V, gains of 250 kΩ and 2.5 MΩ were measured at 100 kHz.

In the transimpedance stage, the feedback impedance (Z) is a parallel resistor and compensation capacitor. An NMOS transistor in triode mode functions as the resistor, enabling gain adjustment through modification of the gate voltage. The differential amplifier is based on a two-stage design [5] with output voltage controlled by a CMFB circuit. This amplifier CMFB works together with the CMFB at the input stage to prevent common-mode current from flowing into the transimpedance stage. The differential photocurrent input to the transimpedance stage is $I_{D1} + I_{D2}/2$. Both photocurrents positively contribute to the TIA output and thus improve overall responsivity.

The last stage is the feedback DC rejection stage. In the feedback loop, a capacitor $C_f$ and operational transconductance amplifier (OTA) work together as a differential integrator. The OTA has a fully differential folded-cascaded structure, similar to that reported [6]. An integrator in the negative feedback circuit amplifies and thus suppresses the low frequency signal. However, within the signal band (95–105 kHz) the feedback loop gain is extremely weak and signals are not affected. Specifically, as shown in Fig. 1, the DC photocurrents $I_{D1}$ and $I_{D2}$ are shunted to transistors M1 and M2 instead of the transimpedance stage. In the steady state, the current flow is $I_{D1} + I_{D2}/2$ for M1 and $I_{D1} - I_{D2}/2$ for M2. Therefore, the feedback loop acts as a closed loop highpass filter (HPF). The cutoff frequency of the HPF is changed by adjusting an external resistor that sets the OTA transconductance.

A dynamic signal analyser (Agilent 35670A) was used for noise and DC rejection measurements. For noise measurement, the photodiode input was blocked and the noise density at the TIA output was measured. The TIA equivalent input current noise density was computed by dividing the measured TIA output noise density by the measured transimpedance gain (1.1 MΩ). Fig. 4 shows the measured noise densities. The measured value at 100 kHz is 2 pA/√Hz, which is about three times greater than the simulated thermal noise value at the same frequency (0.6 pA/√Hz). The measured noise density shows a
1/f falloff, indicating that flicker noise is dominant in the signal band, and may be the reason why measured noise is larger than simulated noise.

The TIA DC rejection capability is limited by the loop gain at low frequency. Therefore, a lower bound on the DC rejection ratio was obtained by taking the ratio of the gains at 100 kHz and 1 Hz. The ratio is 585, corresponding to a TIA DC rejection capability of greater than 55 dB.

**Conclusion:** A fully integrated differential transimpedance amplifier with an on-chip buried double junction photodiode was fabricated for detection of weak modulated signals in the presence of a large DC background. The amplifier achieved gains as high as 2.5 MΩ, a current noise density of 2 pA/√Hz at 100 kHz and a gain of 1.1 MΩ and greater than 55 dB DC rejection capability.

**References**